The University Of Sheffield.

EEE6225 SYSTEM DESIGN

Credits: 15

Course Description including Aims

This unit is concerned with the management of complexity in system design. To learn the basics of structured approach to design of complex systems, students undertake a design project that requires the application of state of the art design tools that help to achieve appropriate error free design structures. The unit is continually assessed at various stages in the design process and these assessments combine to give a grade for the unit.

1. To demonstrate the importance of structured design for complex systems.
2. To provide a working understanding of a standard Hardware Description Language (HDL) which is an aid to structured, error-free design.
3. To provide an appreciation of the special restrictions imposed when using an HDL to design a realisable digital system via synthesis.
4. To give practical exposure to the refinement of a specification through partitioning and design to simulation against a defined set of constraints.

Outline Syllabus

Design Cycle : requirements, specification, design, simulation, implementation, test and integration. **Simulation :** functional v. circuit, concepts, advantages and disadvantages. **Description and Simulation Languages :** Verilog, VHDL & SystemC. **Verilog** : concepts, syntax, behaviour and structure, hierarchy, portability, standards. **Verilog for Synthesis:** The synthesisable subset, standard methodologies, register transfer level (RTL) design. **Design Exercise.**

Time Allocation

12 hours lectures, 12 hours hands-on tutorials, 40 hours of laboratory sessions

Recommended Previous Courses

Basic knowledge of Systems Engineering

Assessment

Assessment is by written report to be submitted by the end of the exercise and various milestones throughout the project. The report will contain the following:

1. a brief report on initial literature survey, current good practice, types of solutions available, solution complexity etc.
2. a copy of the design specification agreed with the supervisor near the start of the exercise, after the initial literature search.
3. a copy of the design schedule used to ensure that the project goals are achieved within the time and resource allowances.
4. a report on the final “product”. This will include a complete description of the final system, simulation results, theoretical performance and an analysis of any deviation from expected

performance.

5. all code written to support the system.

Marks are rewarded on the basis of the following categories:

1. 20% Evidence of a design process throughout the project and in the report.
2. 20% Relationship with existing solutions and quality of choices made in fixing the specifications.
3. 20% Results obtained including achieved performance relative to initial specifications, and relative to expected performance. Analysis of performance.
4. 20% Communication skills in written report.
5. 20% Innovation and initiative.

Recommended Books

Vahid F, Lysecky R	*Verilog for Digital Design*	John Wiley
Zeimer & Peterson	*Introduction to Digital Communications*	McMillan

Objectives

By the end of the module successful students will have demonstrated

1. the specification, design and simulation of a complex digital system using FPGA technology.
2. working in a design team responsible for managing the HDL based design of a digital system.
3. the ability to gather a range of information and literature on a specific algorithm (AES) and prior implementations and to use those to inform the design and implementation of a digital system.
4. the use of industry standard design techniques and design tools.